

1. A semiconductor device provided with:

an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and

15 formed on said inter-layer insulating film; and

a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole.

2. A semiconductor device according to claim 1, wherein the upper surface of said plug is formed to almost the same height as the surface height of said inter-layer insulating film.

3. A semiconductor device according to claim 1, wherein provision is made of:

25 an upper insulating film formed on said

Mr QB

inter-layer insulating film;

a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and

5 a conductive portion which is connected to said plug and formed in said third connection hole.

4. A semiconductor device according to claim 2, wherein provision is made of:

10 an upper insulating film formed on said inter-layer insulating film;

a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and

15 a conductive portion which is connected to said plug and formed in said third connection hole.

5. A semiconductor device according to claim 3, wherein said plug and said conductive portion are the storage node contact portion of a dynamic random access memory.

20 6. A semiconductor device according to claim 4, wherein said plug and said conductive portion are the storage node contact portion of the dynamic random access memory.

25 7. A method of manufacture of a semiconductor device comprising:

a step of forming an inter-layer insulating film on the substrate covering the conductive layer pattern formed on the substrate;

5 a step of forming a first connection hole in the upper layer of said inter-layer insulating film above said conductive layer pattern;

a step of forming a side wall in the side wall of said first connection hole;

10 a step of forming a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and has a smaller diameter than that of the first connection hole in said inter-layer insulating film by self alignment by utilizing said side wall as a mask; and

15 a step of forming the conductive plug in said first connection hole and said second connection hole in a filled state.

8. A method of manufacture of a semiconductor device according to claim 7, wherein:

20 said first connection hole is formed in said first film above said conductive layer pattern and the upper layer of said inter-layer insulating film after forming the first film on said inter-layer insulating film;

25 said second connection hole is formed in

said inter-layer insulating film by the etching using
said first film and said side wall as the mask in a
state where it reaches said conductive layer pattern
from the bottom portion of said first connection hole
5 after forming said side wall on the side wall of said
first connection hole; and

said plug is formed by said side wall and
said plug forming film of the part filled in said first
connection hole and said second connection hole by
10 removing said first film, said side wall and said plug
forming film located at a higher position than the
height of the surface of said inter-layer insulating
film after forming the plug forming film in a state of
filling the internal portions of said first connection
15 hole and said second connection hole.

9. A method of manufacture of a semiconductor
device according to claim 8, wherein:

after the first film is formed on said
inter-layer insulating film, a second film acting as
20 the etching mask when forming said side wall is formed
on the first film; and

the first connection hole is formed
penetrating through said second film in the step of
forming the first connection hole in the said first
25 film above said conductive layer pattern and the upper

10. A method of manufacture of a semiconductor device according to claim 7, further comprising:

a step of forming a third connection hole
in said upper layer insulating film reaching said plug;
and

11. A method of manufacture of a semiconductor device according to claim 8, further comprising:

a step of forming the conductive film
connected to said plug in said third connection hole.

a step of forming the upper layer
insulating film on said inter-layer insulating film;

a step of forming the third connection hole
25 in said upper layer insulating film reaching said plug

and:

a step of forming the conductive film connected to said plug in said third connection hole.

13. A method of manufacture of a semiconductor device according to claim 10, wherein said plug and said conductive film form the storage node contact portion of the dynamic random access memory.

14. A method of manufacture of a semiconductor device according to claim 11, wherein said plug and said conductive film form the storage node contact portion of the dynamic random access memory.

15. A method of manufacture of a semiconductor device according to claim 12, wherein said plug and said conductive film form the storage node contact portion of the dynamic random access memory.

16. A semiconductor device having:
a burying wiring layer for filling a wiring use groove dug in an inter-layer insulating film;
a conductive plug which penetrates through the inter-layer insulating film and connects the burying wiring layer and a connection region beneath the same; and
an inter-layer insulating film covering the wiring layer.

17. A semiconductor device according to claim

18. A semiconductor device according to claim 16, wherein said burying wiring layer constitutes a bit
5 line of a dynamic random access memory.

10 20. A manufacturing method of a semiconductor
device comprising:

a step of filling the wiring use groove by
15 a conductive material;

a step of forming a side wall constituted
20 by the conductive material on an inner wall of the
preparatory contact hole;

25 a step of filling the contact hole by the

a step of flattening an inter-layer insulating film and the conductive material filling the wiring use groove and forming the burying wiring layer;

a step of forming the inter-layer
insulating film covering the burying wiring layer.

22. A method of manufacture of a semiconductor device according to claim 20, wherein the burying wiring layer constitutes the bit line of a dynamic

15 random access memory.